SHENZHEN XINGYUHE CO.,LTD

SPECIFICATIONS

CUSTOMER :

PRODUCT : LCD Module

SAMPLE CODE : JGG12864B04

VER : 1.0

Customer Approved	Confirmed	Designer

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1.GENERAL DESCRIPTION

The JGG12864B04 is a 128X64 DOTS MATRIX LCD module which is fabricated by low power COMS technology. It has an STN panel composed of 128 segments and 64 commons. The LCM can be easily accessed by microcontroller via parallel or serial interface.

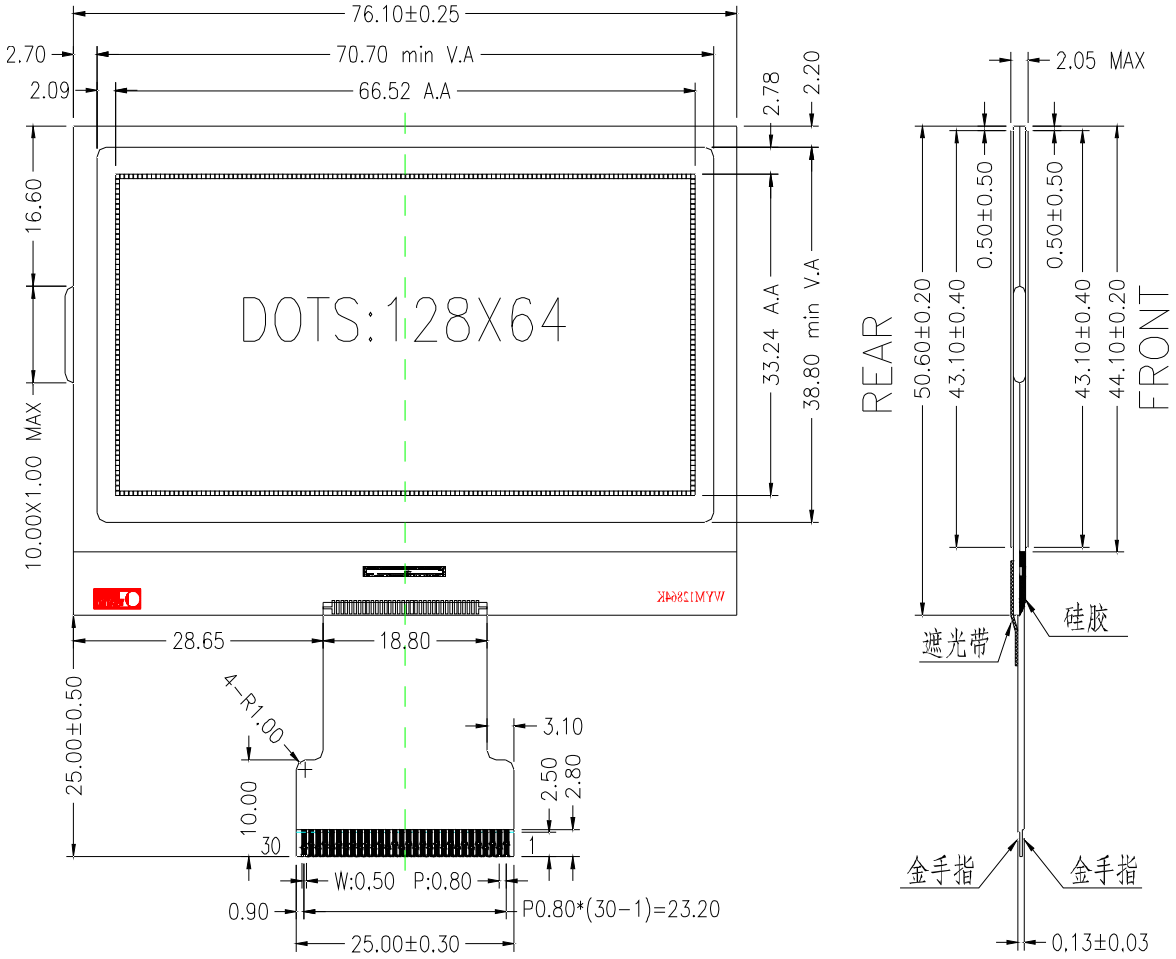
2.FEATURES

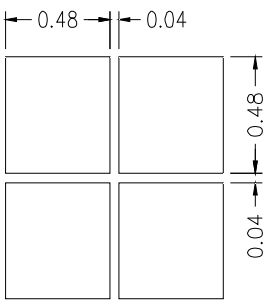
Display Model	TRANSMISSIVE and BLUE type
	STN Mode LCD
Display Format	128X64 DOTS
Input Data	Parallel or serial data input from MPU
Multiplexing Ration	1/65 Duty , 1/9Bias
Viewing Direction	6 O'clock
DRIVER	ST7565P

3.MECHANICAL SPECIFICATION

Item	Specifications	Unit
Module Size(W*H*T)	76.10X（50.60+25.00）X2.05MAX	mm
Viewing Area (W*H)	70.70X38.80	mm
Dot Pitch (W*H)	0.52X0.52	mm
Dot Size (W*H)	0.48X0.48	mm
Active Area (W*H)	66.52X33.24	mm
Number of Dots	128X64	---

4.MECHANICAL DIMENSION





DISPLAY TYPE: STN/BLUE
POLARIZER: TRANSMISSIVE
VIEWING DIRECTION: 6:00-CLOCK
DRIVE METHOD: 1/65DUTY,1/9BIAS
LCM OPERATING VOLTAGE: 3.0V
LCD OPERATING VOLTAGE: 10.3V
OPERATING TEMP: -20 TO 70 Deg.C
STORAGE TEMP: -30 TO 80 Deg.C
CONNECTOR: COG
UNSIGNED TOLERANCE: ±0.20

NO.	SYMBOL
1	NC
2	/CS1
3	/RES
4	A0
5	W/R(R/W)
6	/RD(E)
7	D0
8	D1
9	D2
10	D3
11	D4
12	D5
13	D6
14	D7
15	VDD
16	VSS
17	VOUT
18	C3-
19	C1+
20	C1-
21	C2-
22	C2+
23	V1
24	V2
25	V3
26	V4
27	V5
28	C86
29	P/S
30	NC

5. PIN DESCRIPTIONS

PIN	symbol	voltage	FUCTION
1	NC	--	--
2	/CS1	I	This is the chip select signal. When /CS1 = "L", then the chip select becomes active, and data/command I/O is enabled.
3	/RES	I	When /RES is set to "L," the settings are initialized. The reset operation is performed by the /RES signal level.
4	A0	I	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicates that D0 to D7 are display data. A0 = "L": Indicates that D0 to D7 are control data.
5	W/R(R/W)	I	• When connected to an 8080 MPU, this is active LOW. (R/W) This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When R/W = "H": Read. When R/W = "L": Write.
6	/RD(E)	I	• When connected to an 8080 MPU, this is active LOW. (E) This pin is connected to the /RD signal of the 8080 MPU, and the ST7565P series data bus is in an output status when this signal is "L". • When connected to a 6800 Series MPU, this is active HIGH. This is the 6800 Series MPU enable clock input terminal.
7	D0	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S = "L") : D7 : serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 are set to high impedance. When the chip select is not active, D0 to D7 are set to high impedance.
8	D1		
9	D2		
10	D3		
11	D4		
12	D5		
13	D6		
14	D7		
15	VDD	Power Supply	Power supply
16	VSS	Power Supply	Ground
17	VOUT	O	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD
18	C3-	O	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
19	C1+		
20	C1-		
21	C2-		
22	C2+		
23	V1	Power	power supply liquid crystal drive

24	V2	Supply	
25	V3		
26	V4		
27	V5		
28	C86	I	This is the MPU interface switch terminal. C86 = “H”: 6800 Series MPU interface. C86 = “L”: 8080 MPU interface.
29	P/S	I	This pin configures the interface to be parallel mode or serial mode.
30	NC	--	--

6. MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	5.0	V
	Vout	-0.3	18.0	V
Input Voltage	Vin	VSS-0.3	VDD+0.3	V
Operating temperature	Topr	-20	70	℃
Storage temperature	Tstr	-30	80	℃

7. ELECTRICAL CHARACTERISTICS.

Item		Symbol	Condition	Min	Typ.	Max.	Unit
Supply Voltage		Logic	V_{DD}-GND	-	3.0	-	V
Input voltage	H level	V_{DD}	-	$0.8V_{DD}$	-	V_{DD}	V
	L level	V_{IH}		V_{SS}	-	$0.2V_{DD}$	
LCD Driving Voltage		V_{LCD}		-	10.3	-	V

Note1. The value is measure at following condition; follow same condition to test sample and mass product.

(a)VDD=3.0V (b)1/65Duty ,1/9Bias

8. MODULE FUNCTION DESCRIPTION

1.Timing Characteristics

System Bus Read/Write Characteristics 1 (For the 8080 Series MPU)

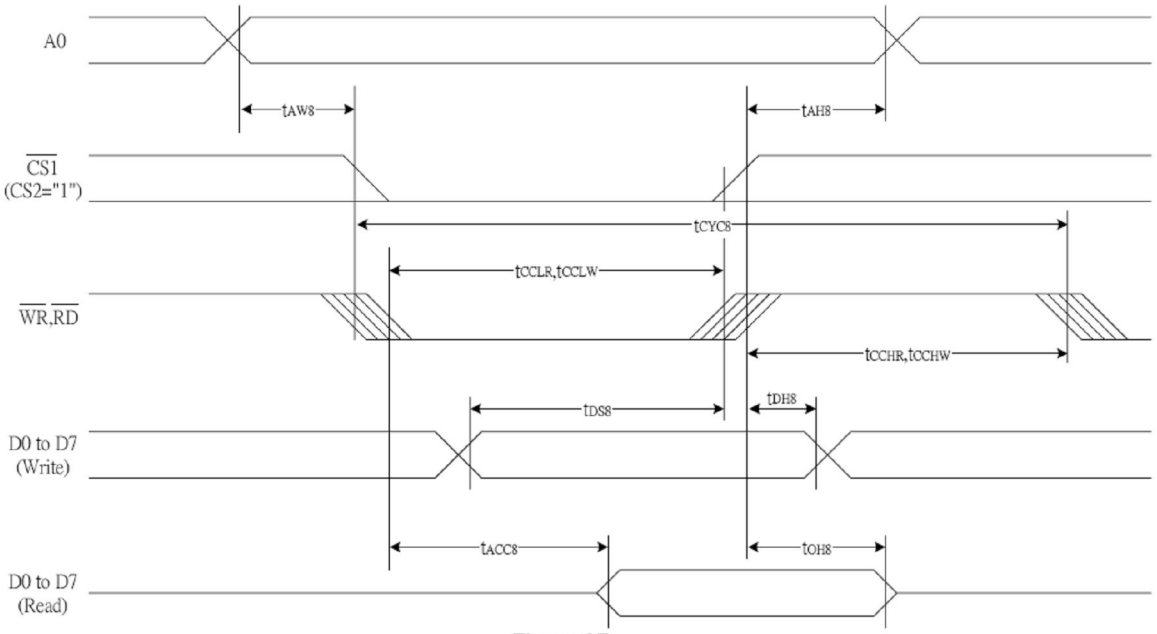


Figure 37

(VDD = 3.3V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	Ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		240	—	
Enable L pulse width (WRITE)	WR	tCCLW		80	—	
Enable H pulse width (WRITE)		tCCHW		80	—	
Enable L pulse width (READ)	RD	tCCLR		140	—	
Enable H pulse width (READ)		tCCHR		80		
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	70	
READ Output disable time		tOH8	CL = 100 pF	5	50	

(VDD = 2.7 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		400	—	
Enable L pulse width (WRITE)	WR	tCCLW		220	—	
Enable H pulse width (WRITE)		tCCHW		180	—	
Enable L pulse width (READ)	RD	tCCLR		220	—	
Enable H pulse width (READ)		tCCHR		180	—	
WRITE Data setup time	D0 to D7	tDS8		40	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	140	
READ Output disable time		tOH8	CL = 100 pF	10	100	

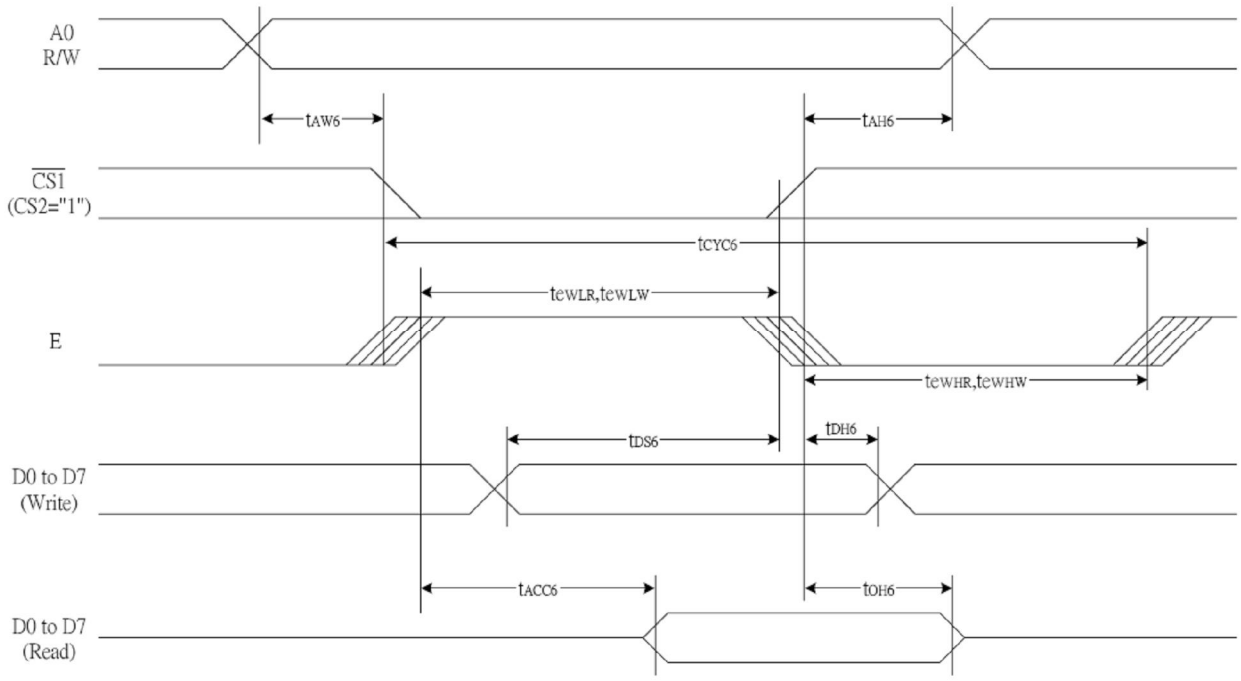
(VDD = 1.8V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	tAH8		0	—	ns
Address setup time		tAW8		0	—	
System cycle time		tCYC8		640	—	
Enable L pulse width (WRITE)	WR	tCCLW		360	—	
Enable H pulse width (WRITE)		tCCHW		280	—	
Enable L pulse width (READ)	RD	tCCLR		360	—	
Enable H pulse width (READ)		tCCHR		280		
WRITE Data setup time	D0 to D7	tDS8		80	—	
WRITE Address hold time		tDH8		0	—	
READ access time		tACC8	CL = 100 pF	—	240	
READ Output disable time		tOH8	CL = 100 pF	10	200	

*1 The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fas (tr +tf) ≦ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≦ (tCYC8 – tCCLR – tCCHR) are specified.

*2 All timing is specified using 20% and 80% of VDD as the reference.

*3 tCCLW and tCCLR are specified as the overlap between /CS1 being “L” (CS2 = “H”) and /WR and /RD being at the “L” leve



System Bus Read/Write Characteristics 2 (For the 6800 Series MPU)

Figure 38

Table 27

(V_{DD} = 3.3 V , Ta = 25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

(VDD = 2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		400	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		220	—	
Enable H pulse width (WRITE)		t_{EWHW}		180	—	
Enable L pulse width (READ)	RD	t_{EWLR}		220	—	
Enable H pulse width (READ)		t_{EWHR}		180	—	
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	140	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	100	

Table 29

(VDD =1.8V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating Min.	Rating Max.	Units
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		640	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		360	—	
Enable H pulse width (WRITE)		t_{EWHW}		280	—	
Enable L pulse width (READ)	RD	t_{EWLR}		360	—	
Enable H pulse width (READ)		t_{EWHR}		280	—	
WRITE Data setup time	D0 to D7	t_{DS6}		80	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	240	
READ Output disable time		t_{OH6}	C_L = 100 pF	10	200	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of VDD as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

The Serial Interface

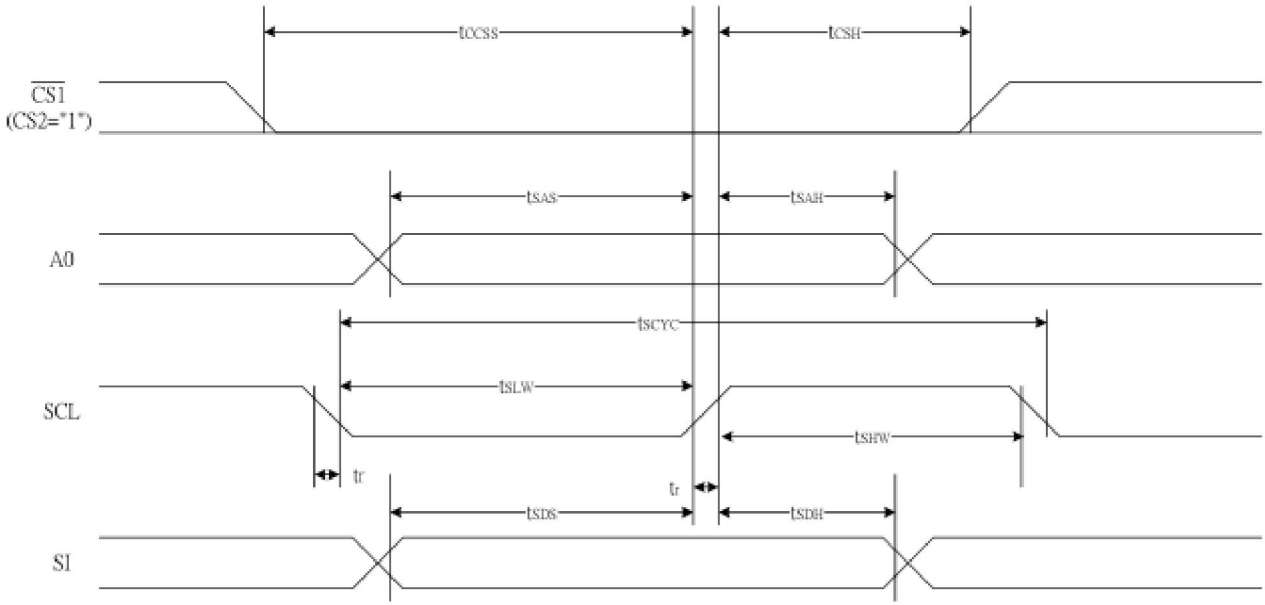


Figure 39

Table 30

(VDD = 3.3V, Ta =25°C)

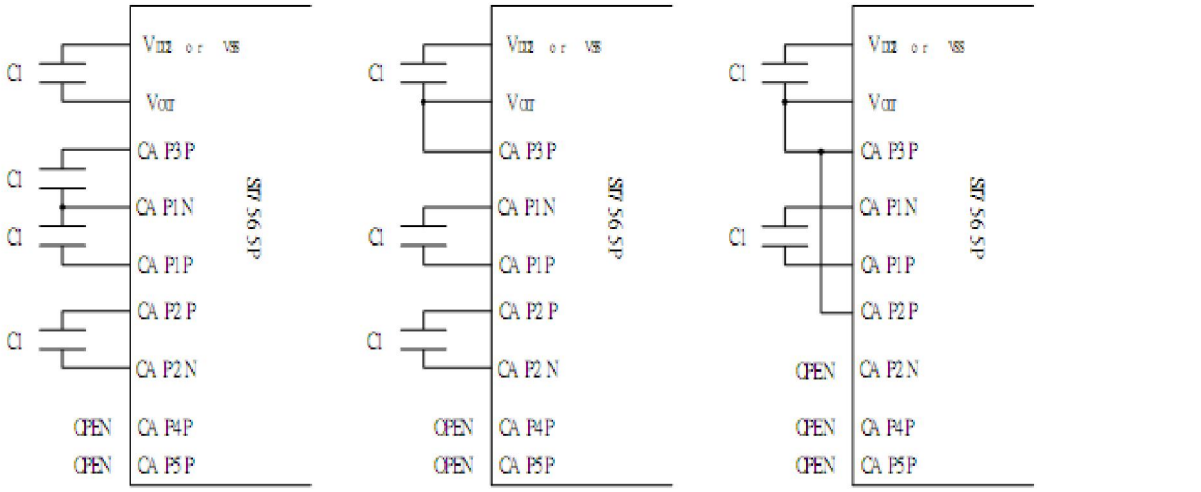
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	Tscyc		100	—	ns
SCL "H" pulse width		Tshw		50	—	
SCL "L" pulse width		TSLW		50	—	
Address setup time	A0	TSAS		20	—	
Address hold time		Tsah		10	—	
Data setup time	SI	Tsds		20	—	
Data hold time		TSDH		10	—	
CS-SCL time	CS	Tcss		20	—	
CS-SCL time		Tcsh		40	—	

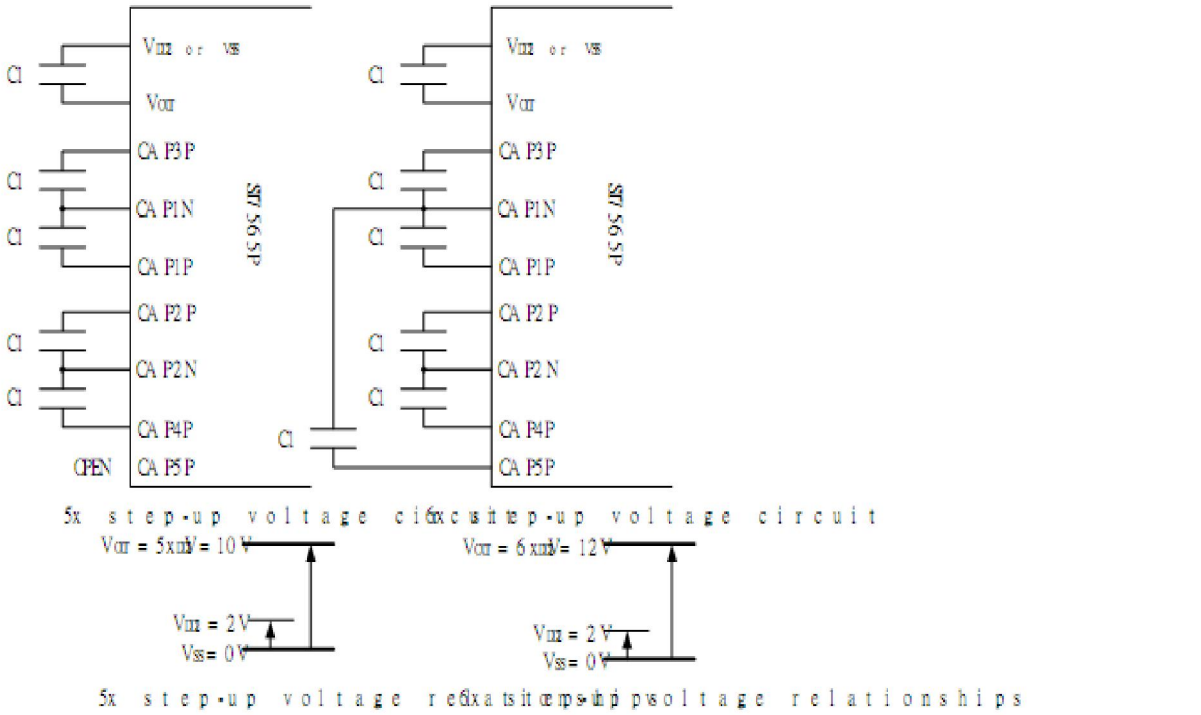
Table 31

(VDD =2.7V , Ta =25°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Serial Clock Period	SCL	Tscyc		120	—	ns
SCL "H" pulse width		TSHW		60	—	
SCL "L" pulse width		TSLW		60	—	
Address setup time	A0	TSAS		30	—	
Address hold time		TSAH		20	—	
Data setup time	SI	TSDS		30	—	
Data hold time		TSDH		20	—	
CS-SCL time	CS	TCSS		30	—	
CS-SCL time		TCSH		60	—	

2. APPLICATION OF LCM





3.COMMAND TABLE

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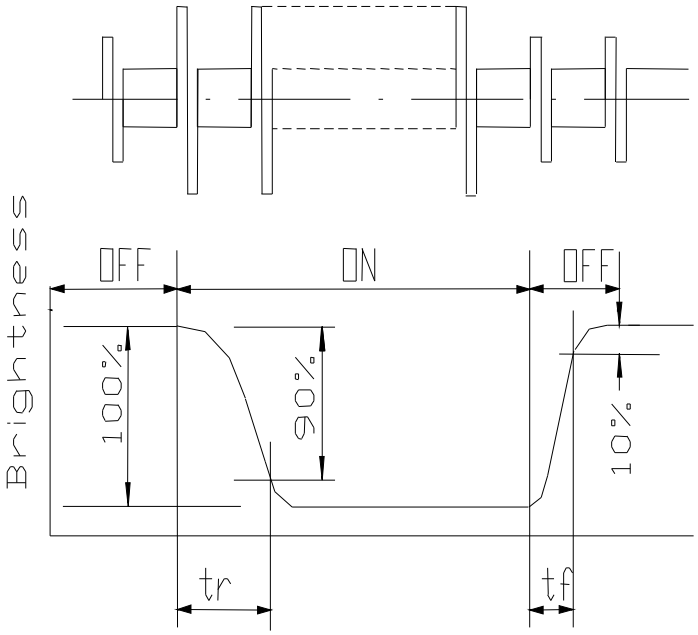
Command	Command Code											Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0	1	0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565R)
(12) Read-modify-write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V_0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V_0 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power save	0	1	0									Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

9. Electro-Optical Characteristics

(1). STN Type

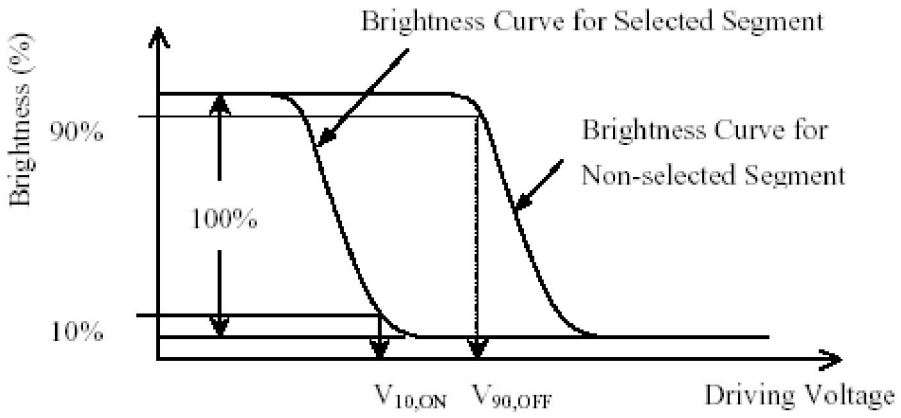
Item	Symbol	Condition	Min	Typ	Max	Units
Contrast	K	θ=0° Φ=0°	5 ： 1	—	—	deg.
Viewing Angle	θ	K=5 Φ=0°	$\theta_2-\theta_1$=30	—	—	deg.
		K=5 θ=10°	Φ=±30	—	—	deg.
Response time	T_{on}	25℃	—	—	250	ms
	T_{off}	25℃	—	—	250	ms

(2). Definition of Optical Response Time



(3). Definition of Driving Voltage (Vlcd)

$Vlcd=(V_{10,ON}+V_{90,OFF})/2$



(4). Definition of Viewing Angle θ and Φ