SHENZHEN XINGYUHE CO.,LTD

SPECIFICATIONS

CUSTOMER :

PRODUCT : LCD Module

SAMPLE CODE : JGG12864B03

VER : 1.0

Customer Approved	Confirmed	Designer

TABLE OF CONTENTS

1.GENERAL DESCRIPTION

The JGG12864B03 is a 128X64 DOTS MATRIX LCD module which is fabricated by low power COMS technology. It has an FSTN panel composed of 128segments and 64 commons. The LCM can be easily accessed by microcontroller via parallel interface.

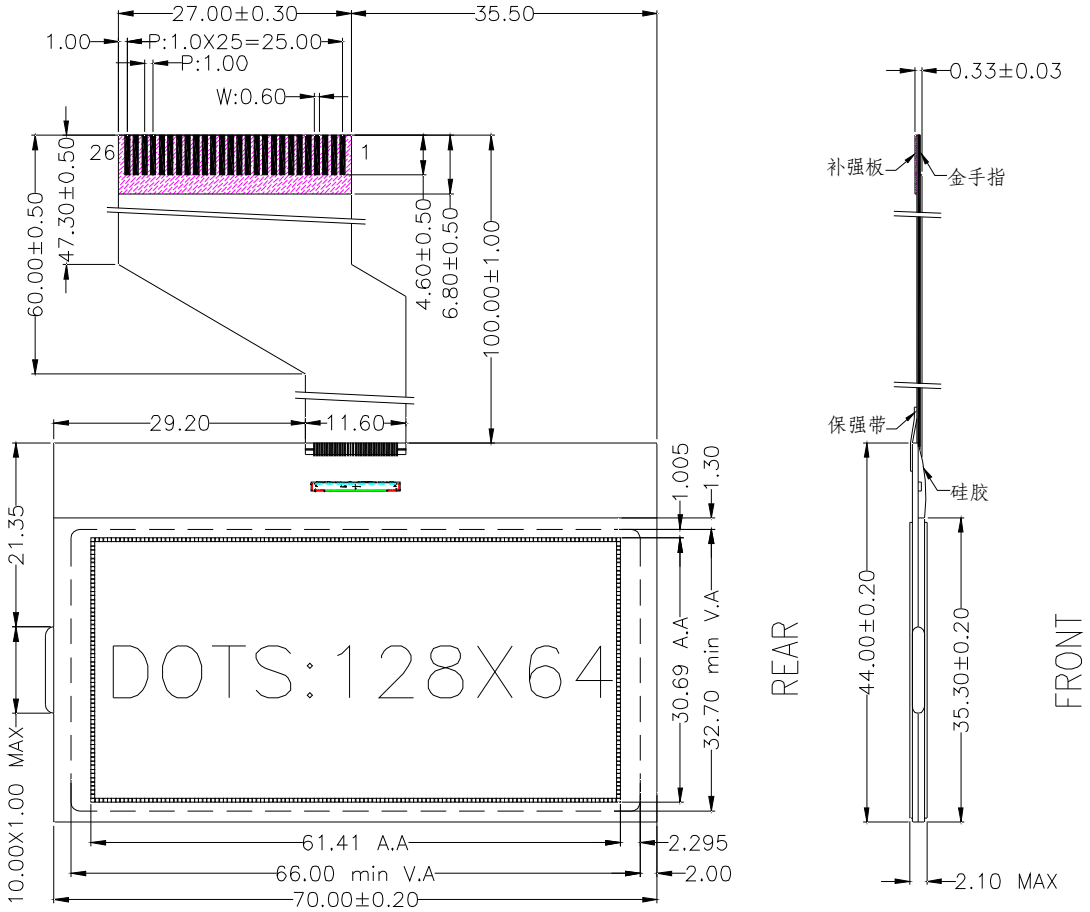
2.FEATURES

Display Model	TRANSFLECTIVE and POSITIVE type
	FSTN Mode LCD
Display Format	128X64 DOTS MATRIX
Input Data	Parallel data input from MPU
Multiplexing Ration	1/65 Duty , 1/9Bias
Viewing Direction	12 O'clock
DRIVER	NT7532

3.MECHANICAL SPECIFICATION

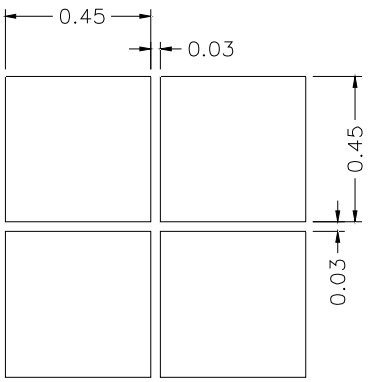
Item	Specifications	Unit
Module Size(W*H*T)	70.00X（44.0+100.00）X2.10MAX	mm
Viewing Area (W*H)	66.00X32.70	mm
Dot Pitch (W*H)	0.48X0.48	mm
Dot Size (W*H)	0.45X0.45	mm
Active Area (W*H)	61.41X30.69	mm
Number of Dots	128X64	---

4.MECHANICAL DIMENSION



NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
PIN	V0	V4	V3	V2	V1	C2−	C2+	C1+	C1−	C3+	VOUT	VSS	VDD	D7	D6	D5	D4	D3	D2	D1	D0	E/RD	RD/WR	A0	RES	CS

DISPLAY TYPE: FSTN/POSITIVE
POLARIZER: TRANSFLECTIVE
VIEWING DIRECTION: 12:00−CLOCK
DRIVE METHOD: 1/65DUTY,1/9BIAS
LCD OPERATING VOLTAGE: 9.4v
LCM OPERATING VOLTAGE: 3.3v
OPERATING TEMP: 0 TO 50 Deg.C
STORAGE TEMP: −20 TO 60 Deg.C
CONNECTOR: COG
UNSIGNED TOLERANCE: ±0.20



5. PIN DESCRIPTIONS

PIN	symbol	voltage	FUCTION
1	V0	SUPPLY	LCD drivers supply voltages
2	V4	SUPPLY	LCD drivers supply voltages
3	V3	SUPPLY	LCD drivers supply voltages
4	V2	SUPPLY	LCD drivers supply voltages
5	V1	SUPPLY	LCD drivers supply voltages
6	C2-	O	Capacitor positive connection pins for voltage converter
7	C2+	O	Capacitor positive connection pins for voltage converter
8	C1+	O	Capacitor positive connection pins for voltage converter
9	C1-	O	Capacitor positive connection pins for voltage converter
10	C3+	O	Capacitor positive connection pins for voltage converter
11	VOUT	I/O	Voltage converter input/output pin
12	VSS	SUPPLY	Power supply (ground)
13	VDD	SUPPLY	Power supply
14	D7	I/O	Input data signal
15	D6	I/O	Input data signal
16	D5	I/O	Input data signal
17	D4	I/O	Input data signal
18	D3	I/O	Input data signal
19	D2	I/O	Input data signal
20	D1	I/O	Input data signal
21	D0	I/O	Input data signal
22	E/RD	I	Read signal input pin, active “L”
23	WR	I	Write signal input pin, active “L”
24	A0	I	Select control data or display for read /write operation
25	RES	I	Reset
26	CS	I	Chip select signal

6. MAXIMUM RATINGS

Item	Symbol	Min	Max	Unit
Supply Voltage	VDD	-0.3	3.6	V
	Vout	-0.3	14.0	V
Input Voltage	Vin	VSS-0.3	VDD+0.3	V
Operating temperature	Topr	0	50	℃
Storage temperature	Tstr	-20	60	℃

7. ELECTRICAL CHARACTERISTICS

(1).

Item		Symbol	Condition	Min	Typ.	Max.	Unit
Supply Voltage		Logic	V_{DD}-GND	-	3.3	-	V
Input cotage	H level	V_{DD}	-	0.8V_{DD}	-	V_{DD}	V
	L level	V_{IH}		V_{SS}	-	0.2V_{DD}	
LCD Driving Voltage		V_{LCD}		-	9.4	-	V

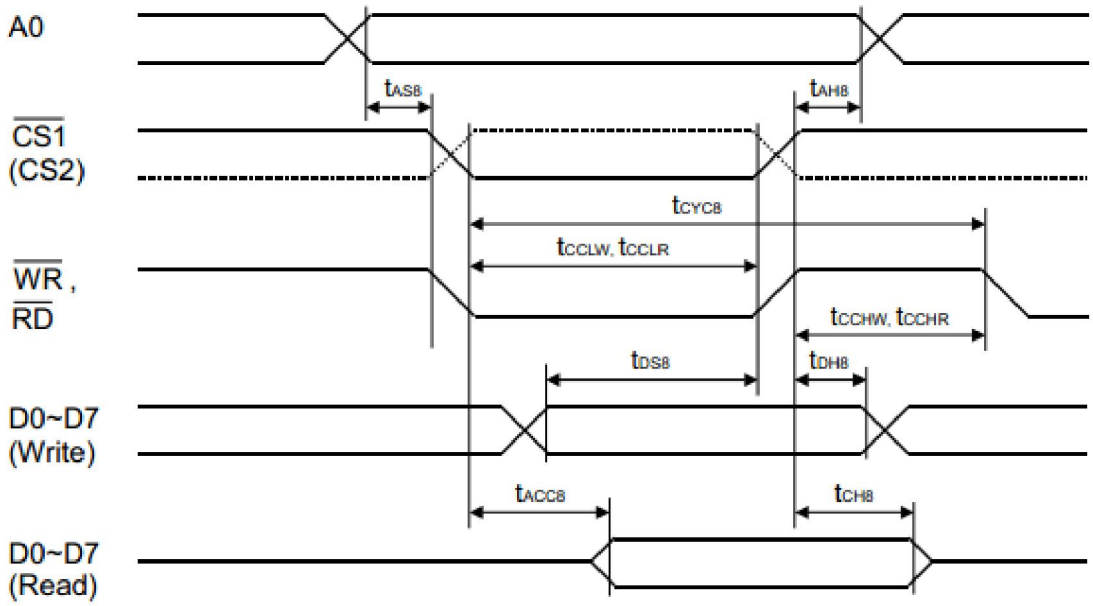
Note1. The value is measure at following condition; follow same condition to test sample and mass product.

(a)VDD=3. 3V (b)1/65Duty ,1/9 Bias

8. MODULE FUNCTION DESCRIPTION

1.Timing Characteristics

System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDD = 2.7 ~ 3.3V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH8}	Address hold time	0	-	-	ns	A0
t_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	300	-	-	ns	
t_{CCLW}	Control low pulse width (write)	90	-	-	ns	$\overline{WR}$
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	$\overline{RD}$
t_{CCHW}	Control high pulse width (write)	120	-	-	ns	$\overline{WR}$
t_{CCHR}	Control high pulse width (read)	60	-	-	ns	$\overline{RD}$
t_{DS8}	Data setup time	40	-	-	ns	D0~D7
t_{DH8}	Data hold time	15	-	-	ns	
t_{ACC8}	$\overline{RD}$ access time	-	-	140	ns	D0~D7, CL = 100pF
t_{CH8}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for write, ($t_r + t_f$) < ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) for read.

*2. All timing is specified using 20% and 80% of VDD as the reference.

*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when $\overline{CS1}$ is low (CS2 is high) and $\overline{WR}$ or $\overline{RD}$ is low.

2.COMMAND TABLE

Table 14. Command Table

Command	A0	RD	WR	Code D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when goes high, and turn off when goes low
(2) Set Display Start Line	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Set Page Address	0	1	0	1	0	1	1	Page Address				B0h to BFh	Set the display data RAM page in Page Address register
(4) Set Column Address	0	1	0	0	0	0	1	Higher Column Address				00h to 1Fh	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Selects normal display (0) or entire display on
(11)Set LCD Bias	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Selects COM output scan direction *: invalid data
(16)Set Power Control	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Selects the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Selects internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static Indicator ON/OFF	0	1	0	0	0	1	0	1	0	1	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation
(22)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(23)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

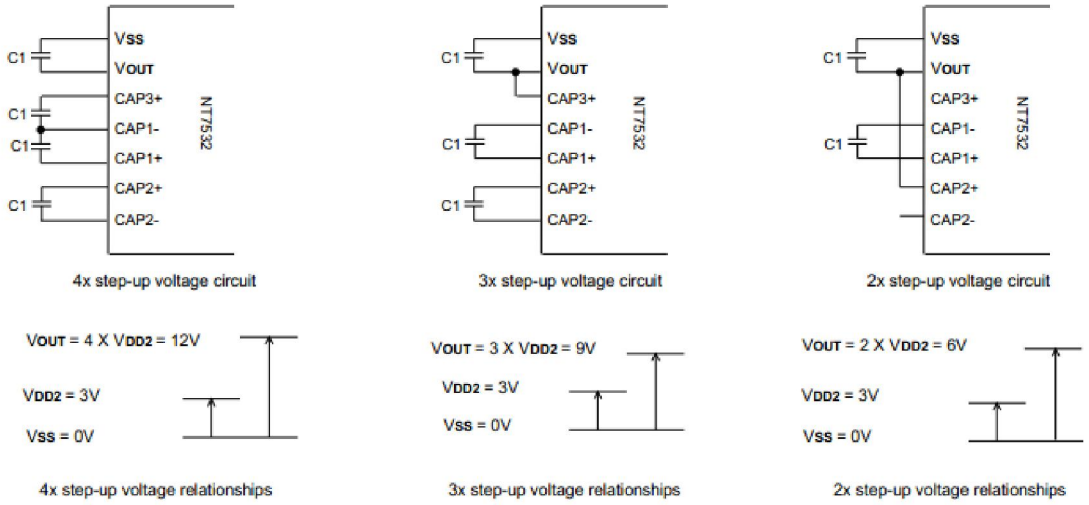
Note: Do not use any other command, or system malfunction may result.

3.APPLICATION OF LCM

The Step-up Voltage Circuits

Using the step-up voltage circuits within the NT7532 chips it is possible to product 4X, 3X, 2X step-ups of the VDD2-VSS2 voltage levels.

Figure. 7

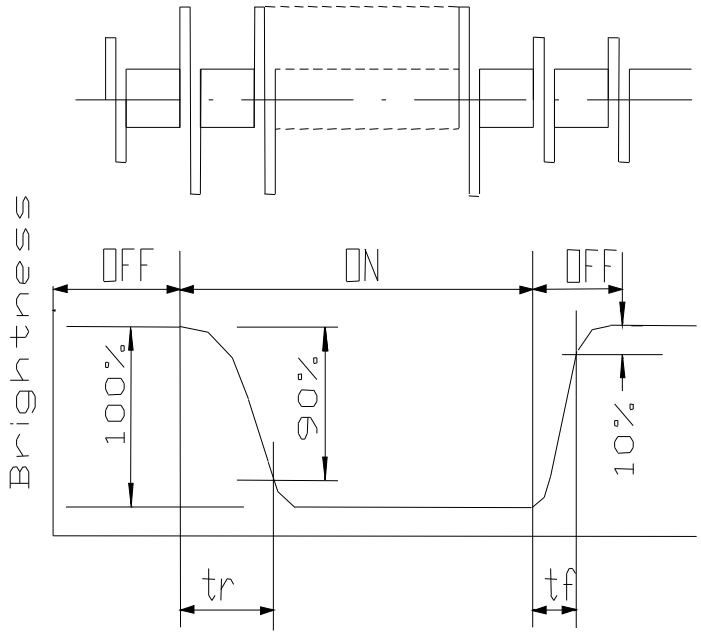


9. Electro-Optical Characteristics

(1).FSTN Type

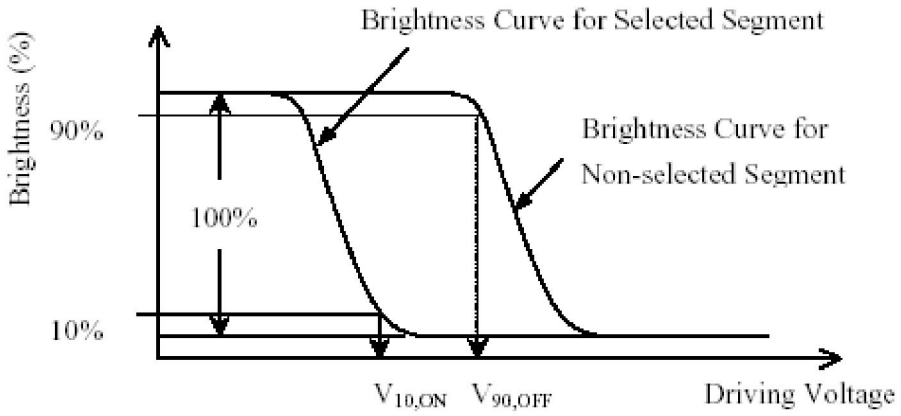
Item	Symbol	Condition	Min	Typ	Max	Units
Contrast	K	θ=0° Φ=0°	5 ： 1	—	—	deg.
Viewing Angle	θ	K=5 Φ=0°	$\theta_2-\theta_1=30$	—	—	deg.
		K=5 θ=10°	$\Phi=\pm 30$	—	—	deg.
Response time	T_{on}	25℃	—	—	250	ms
	T_{off}	25℃	—	—	250	ms

(2). Definition of Optical Response Time



(3). Definition of Driving Voltage (Vlcd)

$$Vlcd=(V_{10,ON}+V_{90,OFF})/2$$



(4). Definition of Viewing Angle θ and Φ